tristate stage are shown in Fig. 12.17-4*b* and *c*.

When memory chips are paralleled for the sake of increasing the number of words, the tristate output stage is enabled and disabled by the chip-select input. Only the output stages on the selected chip are enabled. CMOS gates are also available with a tristate output.

12.18 THE CHARGED-COUPLED DEVICE (CCD)

We have seen that an array of MOSFET devices fabricated on a silicon chip and forming an integrated-circuit dynamic-shift register may serve as a sequential memory. We consider now a different MOS dynamic-shift register sequential memory using the principle of the *charge-coupled device* (*CCD*). While the CCD memory will operate at about the same speed as the MOSFET memory, the CCD memory will dissipate appreciably less power. However, the most important relative advantage of the CCD memory is that it may be fabricated with a density of bits which is of the order of three times the density feasible with MOSFET memories. As we have noted, there is an advantage to using silicon chip "real estate" as economically as possible, since, as the area of the chip increases, there is a corresponding increase of the likelihood of encountering an imperfection in the chip. Hence the improved density possible with CCD devices results in better yields and lower cost. A still further advantage of the CCD device is that it requires a much simpler fabrication procedure involving many fewer operations than is required in MOSFET and in bipolar technology.

The structure of the CCD is represented in Fig. 12.18-1. The device is fabricated on a semiconductor substrate. We have indicated *n*-type silicon for the sake of being specific but *p*-type would serve as well. The substrate is covered with an insulating layer of silicon dioxide and on the oxide an array of closely spaced metal electrodes is arranged. The metal-oxide semiconductor sandwich is reminiscent of the MOSFET structure. Note however, the absence of *p*-type regions which in the MOSFET serve as source and drain.

Let us now consider initially that, while the bottom of the substrate is maintained at ground (0 V), all the metal electrodes are maintained at the same fixed negative voltage, $-V$. As a matter of practice, the spacing between electrodes is extremely small in comparison with their width. (The spacing in Fig. 12.18-1 is grossly exaggerated). Hence, in effect, the metalized layer can be considered to be an equipotential surface at the voltage $-V$. Since the base of the subtrate is an equipotential surface at 0 V, the equipotential surfaces generally are planes parallel to the faces of the structure.

If the voltage $-V$ on the metalization is large enough in magnitude so

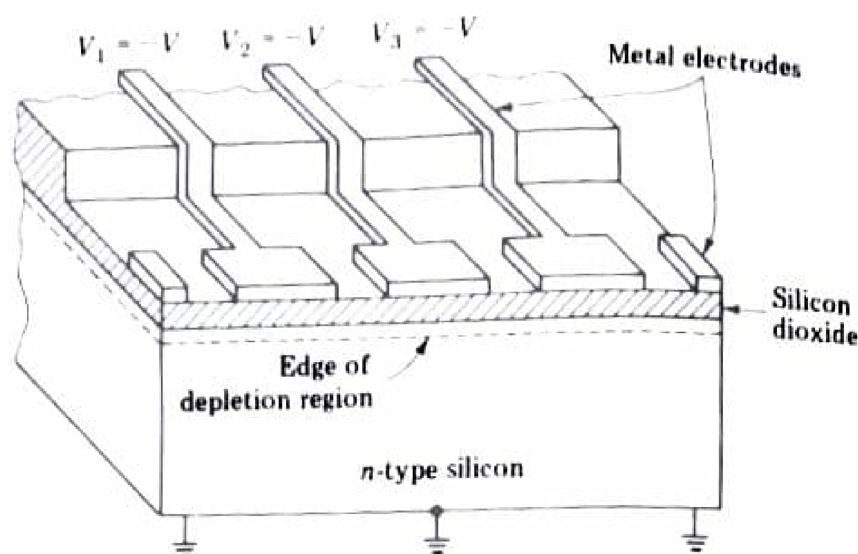

FIGURE 12.18-1
The structure of a charged-coupled device.

that it exceeds the threshold voltage V_T of the substrate, then there will form, under the oxide and adjacent to it, a depletion region. The depletion region is a region from which mobile carriers have been removed. In the present case, the relatively few minority holes present within the substrate will be drawn to the surface of the substrate under the oxide, while the majority carrier—electrons—will be pushed away from the surface. Since predominantly negative charge has been removed from the initially neutral region, the depletion region is left with a positive charge. Lines of electric field which originates from the negative charge on the metal will terminate on this positive charge. The boundary of the depletion region is established when enough positive charge has been provided to allow for the termination of all the electric-field lines. Like a typical equi-potential surface, the depletion region boundary is a plane parallel to the structure surfaces (see Fig. 12.18-1).

Initially, the depletion region shown in Fig. 12.18-1 is devoid of mobile charges. However, as time progresses, holes present in the n-type substrate will diffuse into the depletion region. After a sufficient number of holes have entered the depletion region, there will be formed a conducting layer under the oxide precisely in the manner in which a channel is formed in an MOS device.

Depending on the nature and quantities of impurities in the semiconductor, the absence or presence of defects in the crystal structure of the semiconductor and other factors, the time that elapses between initial depletion and eventual channel generation will be in the range from tenths of seconds to tens of seconds or even longer. In any event, the time is long in comparison with the usual clock interval encountered in a digital system. This feature may seem surprising in view of our experience in connection with MOSFETS. There we noted that, when an appropriate voltage was applied to the gate, a channel formed immediately, i.e., in a matter of tens of nanoseconds. The difference arises from the fact that in the MOSFET, unlike the CCD device, there, there is a source of

minority carriers immediately to the side of the depleted region. Thus in the MOSFET we have, at the outset, a voltage applied between the source and drain. As soon as a voltage is applied to the gate to generate a depleted region, minority carriers from the source and from the drain rush into the depleted region and convert it instead to a conducting channel.

12.19 STORAGE OF CHARGE

Consider now the situation represented in Fig. 12.19-1*a*. Here the voltage on one of the metal electrodes has been made substantially more negative than the voltage on its neighbors; that is, there is a larger negative voltage on electrode 2 than on the others. Accordingly, the depletion region under electrode 2 extends more deeply than under the adjacent electrodes. The boundary of the depleted region now has the form indicated by the dashed line in Fig. 12.19-1*a*.

Qualitative and approximate plots of electrical potential as a function of x, the distance measured horizontally through the substrate, at a number of levels are as shown in Fig. 12.19*b*. At any level which passes through the depletion region the potential, under electrode 2, is *depressed* relative to the potential under its neighboring electrodes. The potential depression is more pronounced for a level AA' which is located closer to the electrodes and is less pronounced for a level CC' located further from the electrodes. We have taken account, in drawing

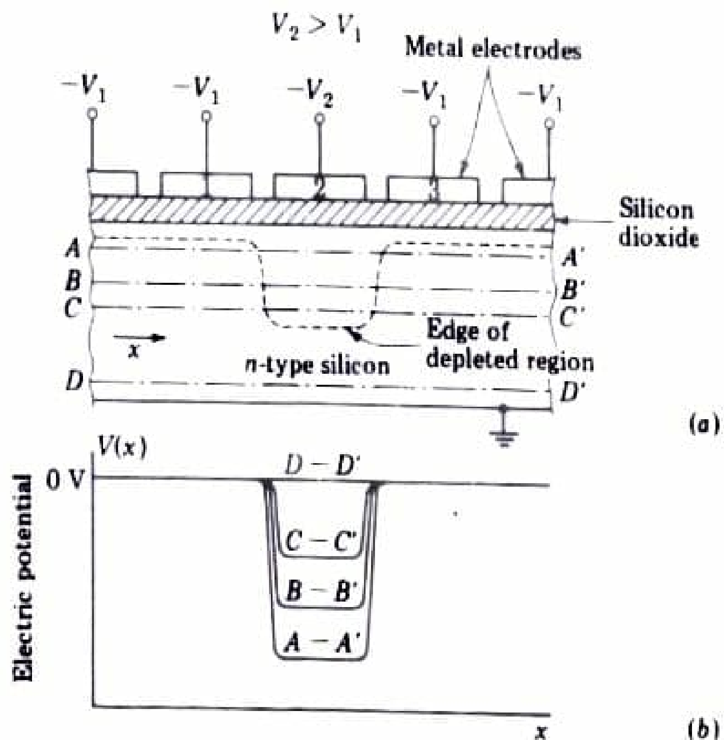

FIGURE 12.19-1
(*a*) The form of the depletion region when one electrode is made more negative that its neighbors. (*b*) The electric potential $V(x)$ through the substrate at various levels.

these plots, that outside the depletion region the substrate is a good conductor, being copiously supplied with majority carriers. Since no current flows, there is no electric field and, hence, no potential difference along the x axis within the n-type substrate.

The reader is now asked to recall that a charged particle of charge q in a field described by a (one-dimensional) potential $V(x)$ has exerted on it a force in the positive x direction given by $f = -q\, dV/dx$. Thus, in Fig. 12.19-1b where the potential is flat ($dV/dx = 0$), there is no force. In the region between electrodes 1 and 2 where dV/dx is negative, the force is to the right, and in the region between electrodes 2 and 3, where dV/dx is positive, the force is to the left. Thus, a positive charge introduced into the depletion region at any level is free to move about only within the "potential well" shown in b.

Finally, then, it appears that the application to a particular electrode of a negative voltage larger in magnitude than is applied to its neighbors generates under that particular electrode an extended depletion region which penetrates more deeply into the substrate. If now we introduce into this region some positive charge (in a manner yet to be described), this charge will be trapped in position. Eventually, this introduced charge will lose its identity because of the diffusion of new carriers into the depletion region as described above. But as long as the charge is identifiable, the presence or absence of such a charge may be used to represent the two logic levels. As we shall now see, there are means by which such trapped charges may be transferred from a position under one electrode to a position under the next, and so on, the whole structure then serving as a shift register.

12.20 TRANSFER OF CHARGE

A mechanism by which charge may be transferred laterally in the CCD is illustrated in Fig. 12.20-1. The CCD device itself, extending laterally in the x direction, appears in Fig. 12.20-1b. We consider initially at time $t = t_0$ that the voltage on electrode k is at $V = -V_2$ while the voltage on all other electrodes is $V = -V_1$. Then there is an extended depletion region under electrode k and a minimal depletion region under all other electrodes. Then, at time $t = t_0$, the voltage $V(x)$ across the substrate, at any level that intersects the extended depletion region, will appear as shown in Fig. 12.20-1c. Here we have assumed that we have devised, by some means, to introduce some positive charge into the depletion region. Somewhat fancifully we have represented the charge as sitting at the bottom of the potential well.

Now, as is indicated in Fig. 12.20-1a, let us arrange that at time $t = t_1$ the voltage on electrode $k + 1$ should also drop to $V = -V_2$. Then the potential profile takes on the appearance shown in Fig. 12.20-1d. The potential barrier to the right of the charge in Fig. 12.20-1c has now been removed. Accordingly, as indicated by the arrow in Fig. 12.20-1d, the charge will diffuse to the right. No charge transport takes place, at least initially, in the reverse direction simply

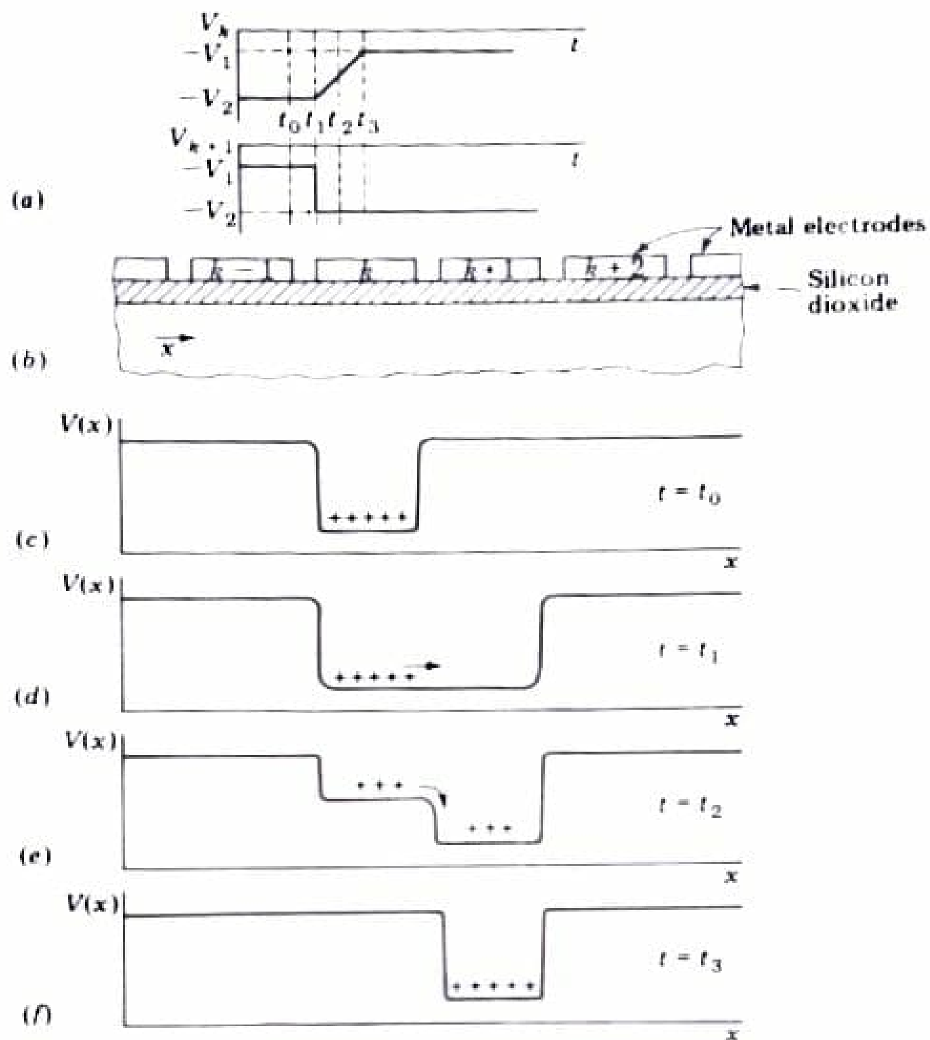

FIGURE 12.20-1
The mechanism of charge transfer. (*a*) The waveform V_k and V_{k+1}. (*b*) The CCD device. (*c*) through (*f*) The potential distributions at times t_0 through t_3 as identified in (*a*). The transfer of the charge is shown.

because there is no charge in the $k + 1$ region. If the voltage profile persisted as shown in Fig. 12.20-1*d*, then eventually the original charge would distribute itself evenly over the k and $k + 1$ region. However, we arrange, as shown by the waveforms of V_k and V_{k+1} in Fig. 12.20-1*a*, that the voltage V_k should now begin to return, relatively slowly, to the value $V_k = -V_1$.

As V_k rises, charge in the k region continues to move to the $k + 1$ region. However, now the mechanism of charge flow is due to a combination of diffusion and the presence of the electric field produced by the potential difference between the regions. Finally at $t = t_3$ and thereafter, as indicated in Fig. 12.20-1*f*, the charge is in the $k + 1$ region, having been transferred there from the k region.

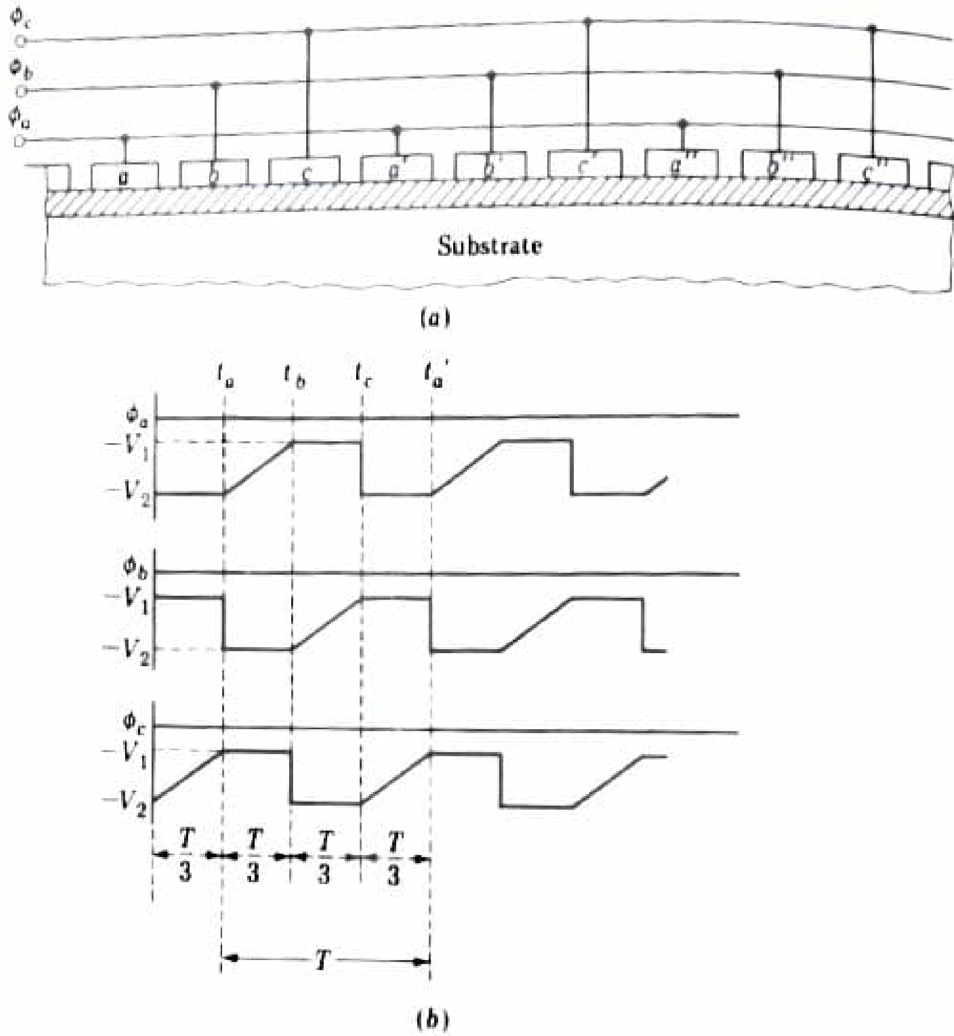

FIGURE 12.20-2
(*a*) The connection of a three-phase clocking waveform to the electrodes of a CCD device. (*b*) The waveforms of the clocking waveform phases.

During the interval from $t = t_1$ to $t = t_2$, while charge is being transferred from the k to the $k + 1$ region, it is necessary that the voltage at electrodes $k - 1$ and $k + 2$ be held at $V = -V_1$ so that no additional depletion region form under these electrodes. If a depletion region formed under electrode $k - 1$, some of the charge in the k region would be transported in the wrong direction. If a depletion region formed under $k + 2$, some of the charge would be transported in the forward direction by two steps rather by one step.

Taking account of the charge-transfer mechanism described, and taking account of the need to ensure that charge is not transferred backward or forward more than one step at a time, we may now consider how to effect a sequence of forward steps in the manner of a shift register. As shown in Fig. 12.20-2*a* every third electrode is connected to a common clocking bus and the three parts ϕ_a, ϕ_b, and ϕ_c of the composite clocking waveform is as in Fig. 12.20-2*b*. The composite clocking waveform has a period T. Each of the parts consists of three subintervals of duration $T/3$. In these subintervals the waveform is at $-V_1$, or at $-V_2$, or is rising from $-V_2$ to $-V_1$. At the time

t_a, ϕ_b has been at $-V_1$ for a full subinterval $T/3$ so that there is certainly no charge under the b electrodes (b, b', b'', etc.). Also ϕ_c has just completed its rise to $-V_1$, as a result of which any charge which might have been under the c electrodes has been completely dumped into the regions under the a electrodes. Accordingly, at $t = t_a$, any charge (or a lack of charge, depending on whether a logic **1** or a logic **0** is being represented) is under the a electrodes. Consider specifically that there is such a charge under the electrode a in Fig. 12.20-2a. Then, during the time interval from t_a to t_b, this charge will be transferred to the region under the b electrode, the process of transfer being completed at time $t = t_b$. At time $t = t_c$ the charge will have been transferred to the region under electrode c. Finally, at time $t = t'_a$, after a total time T the charge which was under a at $t = t_a$ will now be found under a'. Observe, most importantly, that, when the cycle has been completed, charge has been transferred from one region to a second region *three electrodes away*. Thus it takes *three electrodes* to provide for storage and transfer of *one bit*.

We have described a CCD device in which the geometry of the electrodes and insulating oxide layer are such that a three-phase clock is required. This geometry has the difficulty, in the matter of fabrication, that the separation between electrodes is required to be inconveniently small. Other more complicated geometries have been developed which require a four-phase clock, a two-phase clock, and even a single-phase clock.

12.21 INPUT AND OUTPUT ARRANGEMENT

We have seen how a charge trapped in the depletion region under an electrode may be transferred laterally in shift-register fashion. We need to consider briefly how a charge is introduced at the input side and finally detected at the output side.

One method suitable for use in shift-register application is shown in Fig. 12.21-1a. Here, under an opening in the insulating oxide layer we have diffused a p-type region in the n-type substrate. We have also added an additional gating electrode preceding the clocked transfer electrodes. Consider then that the clock phase is such that there is a depletion region under the electrode next to the gating electrode as shown. Then the similarity to the situation that prevails in a MOSFET is rather apparent. If at this time a negative gating voltage is applied, a depletion channel will open under the gate and minority p-type carriers will flow across the channel from the p-type region to the depletion region. When the depletion region has its required complement of charge, the gating voltage is removed. Thereafter the succeeding phases of the clocking waveform transfer this charge laterally, leaving this region under the first transfer electrode available for the next charge.

Correspondingly, the packets of positive charge may be detected, at the end of the register, in the manner indicated in Fig. 12.21-1b. Again a p-type region has been diffused under an opening in the oxide insulation. An external voltage

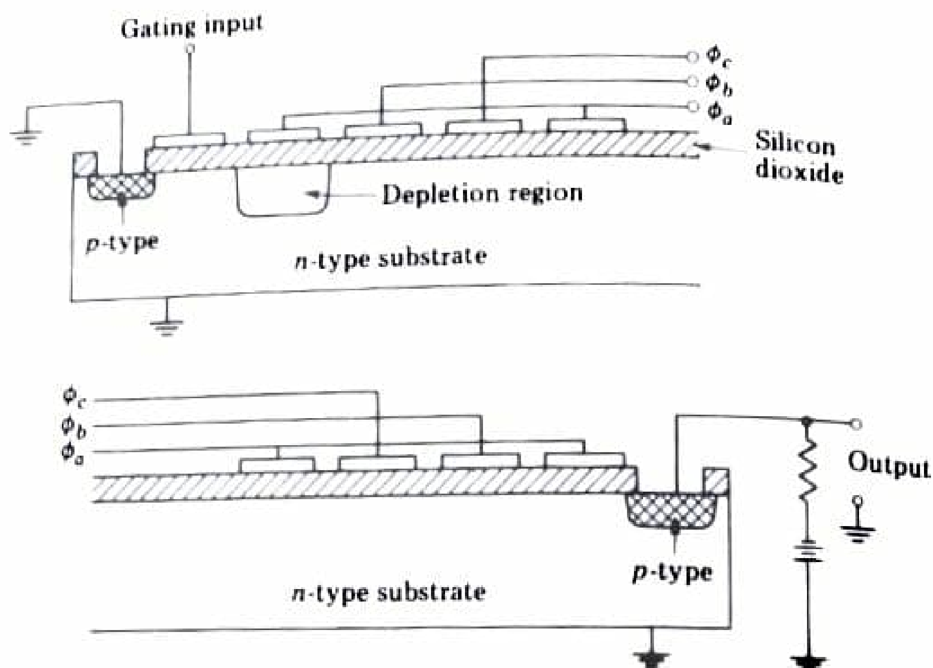

FIGURE 12.21-1
(*a*) A method of injecting a charge into a CCD shift register. (*b*) A method of detecting a charge at the end of a CCD shift register.

source reverse-biases the junction formed between the *n*-type substrate and the *p*-type diffusion. The minority carriers are transferred across this junction just as in the manner in which minority charges are collected by the collector junction of a conventional trasistor. An output voltage is developed across the resistor in series with the reverse-biasing voltage.

The methods described for injecting and collecting charge have the disadvantage, in the matter of fabrication, that high-temperature diffusions into the substrate are required. Other methods that require no such diffusions are also available.

Finally, we must note that the process of charge transfer is not completely efficient. At each transfer of charge, from under one electrode to the next, some charge remains behind. In a long register it is accordingly necessary periodically to provide for refreshing. Refresh amplifier stages are fabricated directly on the substrate of the CCD without involving an inordinate area of the chip.

An example of a CCD memory Typical of the CCD memories presently commercially available is the Intel type 2416 memory. This memory is organized as 64 recirculating shift registers each of 256 bits. We have noted that because of the gradual disappearance of depletion regions a bit cannot be stored in one position indefinitely. There is, accordingly, a minimum time between shifts which must be observed. In the type 2416 this minimum time is 9 μs. The maximum shift rate is 2 MHz. A four-phase clocking waveform is used. Average power dissipation is about 20 μW per bit.